AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below:

1. (Previously Presented) A method of forming a self-gated transistor comprising:

coupling a transistor operable to form a sense signal representative of a current through the self-gated transistor; and

configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor and to enable the transistor responsively to a negative current flow through the transistor.

2. (Previously Presented) The method of claim 1 wherein coupling the transistor operable to form the sense signal representative of the current through the self-gated transistor includes forming the transistor having a main transistor portion and a sense transistor as a sensing portion including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form the sense signal representative of the current through the self-gated transistor.

3. (Original) The method of claim 2 wherein coupling the main transistor portion to the sensing portion includes coupling a drain of the sense transistor to a drain of the main transistor portion and to the drain of the self-gated transistor and also including coupling a gate of the sense transistor to a gate of the main transistor portion and to the gate of the self-gated transistor.

4. (Previously Presented) The method of claim 1 wherein configuring the first circuit of the self-gated transistor to disable the transistor substantially upon the positive current flow through the transistor and to enable the transistor responsively to the negative current flow through the transistor includes coupling a comparator to receive the sense signal wherein the sense signal is positive for the positive current flow and is negative for the negative current flow.

5. (Previously Presented) The method of claim 4 wherein coupling the comparator to receive the sense signal includes coupling a non-inverting input of the comparator to have a negative offset voltage.

6. (Previously Presented) The method of claim 4 wherein coupling the comparator to receive the sense signal includes coupling the comparator to responsively enable the self-gated transistor when the sense signal forms a voltage that is less than a voltage of a source of the self-gated transistor.

7. (Previously Presented) The method of claim 4 wherein coupling the comparator to receive the sense signal includes coupling one of a diode or a resistor between a source of a sense transistor and a source of the self-gated transistor.

8. (Previously Presented) A method of operating a self-gated transistor comprising:

providing an MOS transistor having a main transistor portion and a sensing portion including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form a first sense signal representative of a first current through the main transistor portion;

configuring the self-gate transistor to detect the first sense signal and responsively disable the self-gated transistor;

configuring the self-gate transistor to conduct a second current through the sensing portion as a second sense signal wherein the second current flows in a direction opposite to the first current; and

configuring the self-gate transistor to detect the second sense signal and responsively enable the self-gated transistor.

9. (Previously Presented) The method of claim 8 wherein configuring the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes configuring the self-gate transistor to steer the second current to flow through a diode.

10. (Previously Presented) The method of claim 8 wherein configuring the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes configuring the self-gate transistor to steer the second sense current to flow through a resistor.

11. (Previously Presented) The method of claim 8 wherein configuring the self-gate transistor to detect the first sense signal and responsively disable the self-gated transistor includes coupling an input of a comparator to receive the first sense signal.

12. (Previously Presented) A self-gated transistor comprising:

a transistor having a main transistor portion and a sensing portion wherein the sensing portion is coupled to the main transistor portion to form a sense signal representative of a current through the self-gated transistor, the main transistor portion having a first gate; and

a control circuit coupled to receive the sense signal and drive the first gate to enable the transistor responsively to a first polarity of the sense signal and to disable the transistor responsively to an opposite polarity of the sense signal.

13. (Previously Presented) The self-gated transistor of claim 12 wherein the control circuit includes a comparator having an inverting input coupled to receive the sense signal.

14. (Original) The self-gated transistor of claim 13 wherein the comparator has a non-inverting input coupled to a source of the self-gated transistor.

15. (Original) The self-gated transistor of claim 14 wherein the non-inverting input of the comparator has a negative offset voltage.

16. (Cancelled)

17. (Original) The self-gated transistor of claim 12 further including the sensing portion having a source that is separate from a source of the main transistor portion and a protection circuit coupled to the source of the sensing portion.

18. (Original) The self-gated transistor of claim 12 wherein a source of the main transistor portion is coupled to a source of the self-gated transistor.

19. (Original) The self-gated transistor of claim 12 further including a voltage regulator coupled to provide an operating voltage to the comparator and coupled to a source of the self-gated transistor.

20. (Original) The self-gated transistor of claim 12 further including the self-gated transistor formed in a package having no greater than four leads.

21. (New) The method of claim 1 further including configuring an internal voltage regulator of the self-gated transistor to receive an external voltage having a first value from a voltage source external to the self-gated transistor and regulating the external voltage to form an internal operating voltage having a second value that is less than the first value including configuring the self-gated transistor to use the internal operating voltage to operate the first circuit.